ACCOMMODATION

No TA / DA will be paid to the participants. On prior request, accommodation can be arranged in our college hostel with breakfast & dinner at a nominal fee.

WHO CAN REGISTER?

The programme is open for all college faculty members, industrial persons, research scholars and students. Application can be downloaded from the website www.klnce.edu

REGISTRATION FEE INCLUDES

1) Course Kit
2) Course Materials **(including Lab Manual)**
3) Participation Certificate
4) Working Lunch, Tea & Snacks

REGISTRATION FEE

1) Delegates from Academic Institution and Industry Rs.600/-

2) Research Scholars/Students Rs.500/-

The registration fee should be paid through Demand Draft drawn in favour of "THE PRINCIPAL, K.L.N. COLLEGE OF ENGINEERING" payable at Madurai.

LOCAL TRANSPORTATION

Our college buses are plying on daily over 35 routes from various parts of city. Participants can use these buses to reach K.L.N.C.E. For further information please contact coordinators.

IMPORTANT DATES

Registration form along with D.D should reach us on or before 14th February 2015. Limited spot registration only be allowed.

Detailed Agenda

Day - 1

Session 1: Setting the Perspective

- Analog and Digital - Signals and Systems Perspective
- Inverter - Digital System & Transfer Characteristics
- Quality Metrics- Robustness, Performance, Area & Power
- Conceptualizing the Devices & Networks using VCCS

Session 2: The CMOS Inverter

- The MOSFET *i – v* Characteristics Review
- MOSFET Model - Switching Parameters and Delay
- The CMOS Inverter Design

Session 3 – 4: CMOS Inverter – Hands-on Lab

- Lab 1: PDK Device Characterization – R_{CH}, C_{gs}, C_{db}, C_{sb}, V_T Vs. V_{SB}
- Lab 2: CMOS Inverter Schematic Capture and Characterization – V_{OH}, V_{IL}, V_{OL}, V_{IL}, NM, V_{SP}, t_{pd}, P_{dyn}
- Lab 3: Basic Layout Concepts – Inverter Layout, DRC, LVS, XRC and Back Annotation, Corner Simulation

Day - 2

Session 5: ASIC Standard Cell Layout Design

- Why Standard Cells and what is Standard about them?
- Design of Standard Cell Template

Session 6: Inverter Standard Cell – Hands-on Lab

- Lab 4: Standard Cell Layout for Inv 1X, 2 X drive strengths
- Lab 5: Schematic and Layout Design of NAND2 Gate

Session 7: Design of Sequential Elements

- Lab 6: Conceptualizing the D Latch and Schematic Design, Characterization – $T_{SET\ UP}$, T_{HOLD}

Session 8: Introduction to Analog Circuit Design

- Inverter as an Amplifier (Basic Gain Stage) – Review
- Lab 7: Characterizing MOSFET Analog Parameters
- Lab 8: Characterizing the Basic CS Amplifier

CORRESPONDENCE

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Assistant Professor

Department of ECE
K.L.N. College of Engineering
Pottapalayam – 630 611. Madurai, Tamilnadu

A Two day National Workshop

On

Digital Custom IC Design

using

Cadence Systems Custom Design Flow

(Bridging Concepts to Practices)

19-02-2015 & 20-02-2015
(Thursday & Friday)

Chairman
Dr.A.V.Ramprasad, Principal

Convener & H.O.D - ECE
Dr.V.Kejalakshmi

Coordinators
Mr.N.Janakiraman
Mr.D.Anand

Organized by

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

K.L.N.COLLEGE OF ENGINEERING
Pottapalayam - 630 611
Madurai District.
Phone: 0452 2090971, 2090972
URL : www.klnce.edu

in collaboration with

Entuple Technologies Private Limited
Bangalore

ABOUT THE INSTITUTE

K.L.N. College of Engineering has been the first self-financing co-educational Engineering College started in Madurai in 1994. The College has been affiliated to Anna University and approved by All India Council for Technical Education (AICTE). The College is located in the south eastern outskills of Madurai and is 11Km away from Madurai city. The college runs 7 undergraduate engineering programs and 7 Master Programs including M.E. Communication Systems.

DEPARTMENT OF ECE

The Department of ECE was started in 1994. The Department has adequate infrastructure with spacious classrooms, conference halls and well developed nine laboratories having the advanced designing tools like MATLAB, Orcad P-Spice, Xilinx, Mentor Graphics, IE3D, ADS, AnSoft, LabView and modernized equipments like spectrum analyzer, network analyzer, microwave power meter, GPS kit. The department initiates the U.G., P.G. & research projects in Embedded Systems through the Centre for Embedded Systems which is based on the collaboration of institution & Embedded industry. The department library has over 1500 books and magazines and journals. AICTE, New Delhi has sanctioned fund as under MODROB scheme for modernizing Microwave Lab and DSP lab of this department.

ABOUT THE ENTUPLE TECHNOLOGIES

Entuple Technologies which aims to bring the most advanced technology of the engineering industry to universities worldwide. Entuple Technology team with its experience in different sectors such as Telecommunication, Defense and Aerospace, Power & Utility OEMs, Research & Academia has joined together to build a world class team of Next Generation Solution Enablers in system design technologies. Entuple is committed to bridge the ever growing gap in the industry by bringing in expertise to meet technological challenges by introducing cutting edge platforms, tools and solutions. Please refer www.entuple.com for more details.

ABOUT THE WORKSHOP

The objective of the workshop is to provide hands – on *walk through* to the participants on practical CMOS Circuit design, bridging the theoretical concepts taught/ learnt at the undergraduate and graduate courses of ECE Engineering to the application perspective and practices. The workshop focuses primarily on the ASIC Standard Cell Library Design Methodology starting from the basic CMOS Logic Gate Design covering schematic design, layout, physical verification, parasitic extraction, back annotation and post layout simulation/ characterization of the gate, followed by the design and characterization of a an application circuit such as a Ring Oscillator and its characterization and an insight into the PDK Device Characterization using the CADENCE Custom Design Flow.

TOPICS

1. Quality Metrics of a Digital Gate
2. MOSFET Review and Characterization
3. CMOS Inverter Design and Characterization
4. Ring Oscillator Design and Characterization
5. Insight into the ASIC Standard Cell Library Design
6. Insight into the CMOS Analog Custom Design

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REGISTRATION FORM

Name :

Qualification :

Designation :

Experience :

Department :

Organization :

Address for Communication :

Phone No. :

Mobile No. :

E-mail id :

Accommodation required : Yes ☐ **No** ☐

Date: **Signature of the Applicant**