ACCOMMODATION

No TA / DA will be paid to the participants. On prior request, accommodation can be arranged in our college hostel with breakfast & dinner at a nominal fee.

WHO CAN REGISTER?

The programme is open for all college faculty members, industrial persons, research scholars and students. Application can be downloaded from the website www.klnce.edu

REGISTRATION FEE INCLUDES

- 1) Course Materials
- 2) Participation Certificate
- 3) Working Lunch, Tea & Snacks

REGISTRATION FEE

- 1) Delegates from Academic Institution and Industry Rs.700/-
- 2) Research Scholars/Students Rs.600/-

The registration fee should be paid through Demand Draft drawn in favour of "THE PRINCIPAL, K.L.N. COLLEGE OF ENGINEERING" payable at Madurai.

LOCAL TRANSPORTATION

Our college buses are plying on daily over 35 routes from various parts of city. Participants can use these buses to reach K.L.N.C.E. For further information please contact coordinators.

IMPORTANT DATES

Registration form along with D.D should reach us on or before 9th February 2016. Limited spot registration only be allowed.

> EC 6612 – VLSI Design Laboratory FPGA Based Experiments

COURSE CONTENT

Day-1

- 7-Series Architecture Overview
- Lab 1: Vivado Design Flow

Use Vivado IDE to create a simple HDL design. Simulate the design using the XSIM HDL simulator available in Vivado design suite. Generate the bit-stream and verify in hardware.

- Synthesis Technique
- Implementation and Static Timing Analysis
- Lab 2: Implementing the Design Implement the synthesized design of previous lab, perform timing analysis, generate bit-stream, download the bit-stream and verify
- the functionality.
- Xilinx Design Constraints
- Hardware Debugging
- Lab 3: Hardware Debugging

Use Mark Debug feature and also available Integrated Logic Analyzer (ILA) core (available in IP Catalog) to debug the hardware

Day-2

- Introduction to HLS
- Using Vivado HLS
- Lab 4: Creating Project and Understanding Reports

Experience a basic design flow of Vivado HLS and review generated output.

- Improving Performance
- Lab 5: Optimizing Performance through Pipelining

Use pipelining technique to improve performance.

- Data Types
- Creating a Processor System
- Demonstration of Audio System

Use IP-XACT export capability of Vivado HLS to generate an IP and integrate the generated core in an embedded system developed using IP Integrator. A Two day National Workshop On

"Xilinx Vivado Design Flow & High Level Synthesis Flow Using Zyng"

(EC 6612 – VLSI Design Laboratory FPGA Based Experiments)

> 11-02-2016 & 12-02-2016 (Thursday & Friday)

Chairman Dr.A.V.Ramprasad, Principal

Convener & H.O.D - ECE Dr.V.Kejalakshmi

> Coordinators Dr.N.Janakiraman Mr.D.Anand



Organized by

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

In Association with





K.L.N.COLLEGE OF ENGINEERING Pottapalayam - 630 612 Madurai District. Phone: 0452 2090971, 2090972 URL : www.klnce.edu

ABOUT THE INSTITUTE

K.L.N. College of Engineering has been the first self-financing co-educational Engineering College started in Madurai in 1994. The College has been affiliated to Anna University and approved by All India Council for Technical Education (AICTE). The College is located in the south eastern outskills of Madurai and is 11Km away from Madurai city. The college runs 7 undergraduate engineering programs and 7 Master Programs including M.E. Communication Systems.

DEPARTMENT OF ECE

The Department of ECE was started in 1994. The Department has adequate with infrastructure spacious classrooms, conference halls and well developed nine laboratories having the advanced designing tools like Xilinx Vivado System Edition, Mentor Graphics Front-end & Back-end design suites, LabView, MATLAB, ADS, AnSoft, Orcad P-Spice and modernized equipments like Analog discovery kit, Microwave power meter, Spectrum analyzer, Network analyzer. The department initiates the U.G., P.G. & research projects in Embedded Systems through the Centre for Embedded Systems which is based on the collaboration of institution & embedded industry. AICTE, New Delhi has sanctioned fund as under MODROB scheme for modernizing Microwave Lab and DSP lab of this department. The department library has over 1500 books and magazines and journals.



About CoreEL University Program

CoreEL University Program provides Eco-System support to Indian Academia in Engineering Higher Education, in the field of embedded systems thereby enabling the delivery of quality education. CoreEL university achieves this by providing state of the art products from XILINX, MENTOR GRAPHICS, MATLAB, ANSYS, VxWorks (WIND RIVER), Speedgoat (Rapid Controller Prototyping, Hardware-in-the-Loop simulation, and deployment), PCB Design Tools from Mentor Graphics, Analog Discovery Kits from Digilent (Analog Discovery kit can replace the conventional regulated power supply, Function Generator, Oscilloscope, and smaller parts like Bread board etc with one portable, compact and power effective and low cost solution!) to universities Multiyear application engineering support on these products Faculty and student training, providing industry specific inputs to update the curriculum and helping universities set up Centers of Excellence in Embedded Systems arena.

RESOURCE PERSONS

CoreEL Technologies, Bangalore

Ms.Sadiya, National Manager Mr.G.Prakash, Technical Support Specialist Mr.V.Senthilmurugan, Zonal Manager Mail: upt@coreel.com Cell No: +91-7708233133

CORRESPONDENCE

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- 2) **Mr.D.Anand** (Mobile: 80982 60007) E-Mail: anand.duraiswamy@gmail.com Assistant Professor

Department of ECE K.L.N. College of Engineering Pottapalavam – 630 612. Madurai, Tamilnadu. A Two day National Workshop On "Xilinx Vivado Design Flow & High Level Synthesis Flow Using Zynq" (EC 6612 – VLSI Design Laboratory FPGA Based Experiments) 11-02-2016 & 12-02-2016

(Thursday & Friday)

REGISTRATION FORM

Name	:	
Qualification	:	
Designation	:	
Experience	:	
Department	:	
Organization	:	
Address for		
Address for	:	
Communication	on	
Phone No.	:	
Mobile No.	:	
E-mail id	:	
Accommodat	Accommodation required : Yes No	
Date:	Signature of the Applicant	