ACCOMMODATION

No TA / DA will be paid to the participants. On prior request, accommodation can be arranged in our college hostel with breakfast & dinner at a nominal fee.

WHO CAN REGISTER?

The programme is open for all college faculty members, industrial persons, research scholars and students. Application can be downloaded from the website www.klnce.edu

REGISTRATION FEE INCLUDES

1) Course Kit
2) Course Materials **(including Lab Manual)**
3) Participation Certificate
4) Working Lunch, Tea & Snacks

REGISTRATION FEE

1) Delegates from Academic Institution and Industry Rs.500/-

2) Research Scholars/Students Rs.400/-

The registration fee should be paid through Demand Draft drawn in favour of "THE PRINCIPAL, K.L.N. COLLEGE OF ENGINEERING" payable at Madurai.

LOCAL TRANSPORTATION

Our college buses are plying on daily over 35 routes from various parts of city. Participants can use these buses to reach K.L.N.C.E. For further information please contact coordinators.

IMPORTANT DATES

Registration form along with D.D should reach us on or before 10th January 2018. Limited spot registration can be allowed.

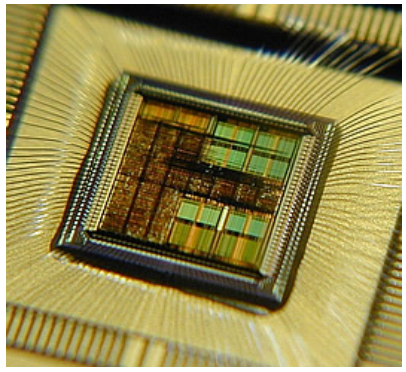
PROGRAM SCHEDULE

DAY-1:-

09:00 - 09:30 – Registration
09:30 - 09:45 – Inauguration
09:45 - 10:30 – Presentation on VLSI FPGA Design Flow
10:30 - 10:45 – Tea Break
10:45 - 12:45 – Presentation & Demonstration on Xilinx Tools – Vivado ISE Simulator, High Level Synthesizer (HLS), Logic Analyzer & FPGA Configurations
12:45 - 01:30 – Lunch Break
01:30 - 03:00 – Hands on - 8 bit Adders & 4 bit Multipliers – Vivado ISE Simulator & Synthesizer (XST)
03:00 - 05:00 – Hands on - Decoders & Multiplexers – Logic Analyzer & FPGA Configurations

DAY-2:-

09:10 - 09:45 – Presentation on VLSI ASIC Design Flow
09:45 - 10:30 – Presentation on Cadence' Front-end & Back-end Tools
10:30 - 10:45 – Tea Break
10:45 - 11:45 – Demonstration on CMOS Inverter design using Cadence' tools – Virtuoso & Innovus implementation system
11:45 - 12:45 – Hands on - Cadence' Tools – Virtuoso Platform
12:45 - 01:30 – Lunch Break
01:30 - 04:25 – Hands on – Cadence' Tools
04:25 - 04:45 – Feedback and Conclusion



Two-Day Workshop on

"VLSI Design Laboratory"

11-01-2018 & 12-01-2018
(Thursday & Friday)

Chairman
Dr.A.V.Ram Prasad, Principal

Convener & H.O.D - ECE
Dr.V.Kejalakshmi

Coordinators
Dr.N.Janakiraman
Mr.D.Anand

Organized by
Department of Electronics & Communication Engineering
K.L.N.COLLEGE OF ENGINEERING

Pottapalayam - 630 612
Sivagangai District.
Phone: 0452 2090971, 2090972
Fax: 0452 2090970
URL : www.klnce.edu

ABOUT THE INSTITUTE

K.L.N. College of Engineering has been the first self-financing co-educational Engineering College started in Madurai in 1994. The College has been affiliated to Anna University and approved by All India Council for Technical Education (AICTE). The College is located in the south eastern outskills of Madurai and is 11Km away from Madurai city. The college runs 7 undergraduate engineering programs and 7 Master Programs including M.E. Communication Systems.

DEPARTMENT OF ECE

The Department of ECE was started in 1994. The Department has adequate infrastructure with spacious classrooms, conference halls and well developed ten laboratories having the advanced designing tools like Xilinx Vivado, Xilinx System Edition, Mentor Graphics, MATLAB, Orcad P-Spice, IE3D, ADS, AnSoft, LabView and modernized equipments like spectrum analyzer, network analyzer and microwave power meter. The department initiates the U.G., P.G. & research projects in Embedded Systems through the Centre for Embedded Systems which is based on the collaboration of institution & Embedded industry. The department library has over 1500 books and magazines and journals. AICTE, New Delhi has sanctioned fund as under MODROB scheme for modernizing Microwave Lab and DSP lab of this department.

OBJECTIVES OF THE WORKSHOP

THEORY SESSION:-

- Introduction to VLSI Design Flow
- Front-end Design Flow with Xilinx Vivado System Edition & Cadence tools
- Basics of FPGA, Overview of Xilinx & Altera Products & its Architectural overview
- Back-end Design Flow with Cadence tools
- **Discussion on Academic syllabus EC6612 – VLSI Design Laboratory for U.G. students**

DEMONSTRATION & HANDS-ON SESSION:-

- Simulation using Xilinx Vivado ISE & Cadence' Incisive Simulator
- Synthesis using Xilinx Synthesis Tool & Cadence' Genus Synthesis Solution
- Data Configuration in Xilinx & Altera FPGAs
- CMOS Inverter design using Cadence' tools
- Schematic Entry and SPICE simulation of MOS differential amplifier

CORRESPONDENCE:

1) Dr.N.Janakiraman (Mobile: 98944 24665)
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Professor

2) Mr.D.Anand (Mobile: 80982 60007)
E-Mail: anand.duraiswamy@gmail.com
Assistant Professor

Department of ECE
K.L.N. College of Engineering
Pottapalayam – 630 612.
Madurai, Tamilnadu.

Two-Day Workshop on "VLSI Design Laboratory"

11-01-2018 & 12-01-2018
(Thursday & Friday)

REGISTRATION FORM

Name :

Qualification :

Designation :

Experience :

Department :

Organization :

Address for Communication :

Phone No. :

Mobile No. :

E-mail id :

Accommodation required : Yes ☐ No ☐

Date: **Signature of the Applicant**