ACCOMMODATION

No TA / DA will be paid to the participants. On prior request, accommodation can be arranged in our college hostel with breakfast & dinner at a nominal fee.

WHO CAN REGISTER?

The programme is open for all college faculty members, industrial persons, research scholars and students. Application can be downloaded from the website www.klnce.edu

REGISTRATION FEE

1) Delegates from Academic Institution and Industry Rs.500/-
2) Research Scholars/Students Rs.400/-

The registration fee should be paid through Demand Draft drawn in favour of "THE PRINCIPAL, K.L.N. COLLEGE OF ENGINEERING" payable at Madurai.

LOCAL TRANSPORTATION

Our college buses are plying on daily over 35 routes from various parts of city. Participants can use these buses to reach K.L.N.C.E. For further information please contact coordinators.

IMPORTANT DATES

Registration form along with D.D should reach us on or before 11th February 2020. Limited spot registration only be allowed.

CORRESPONDENCE

1) **Dr.N.Janakiraman** (Mobile: 98944 24665)
E-Mail: janakiramanforu@yahoo.com
Professor

2) **Mr.D.Anand** (Mobile: 80982 60007)
E-Mail: anand.duraiswamy@gmail.com
Assistant Professor

Department of ECE
K.L.N. College of Engineering
Pottapalayam – 630 612. Madurai, Tamilnadu.

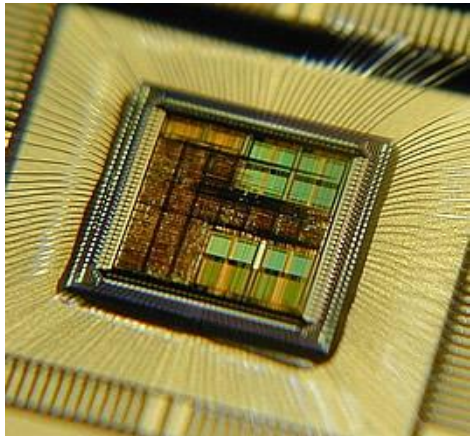
OBJECTIVES OF THE WORKSHOP

THEORY SESSION:-

- Introduction to VLSI Design Flow
- Front-end Design Flow with Xilinx Vivado System Design & Cadence digital suite tools
- Basics of MOSFET and its analysis
- Basics of FPGA and Overview of Xilinx products and its Architectural
- Back-end Design Flow with Cadence Digital System Design tools
- **Discussion on Academic syllabus EC 8661 – VLSI Design Laboratory for U.G. students**

DEMONSTRATION & HANDS-ON SESSION:-

- Simulation using Xilinx ISE System Design & Vivado Design Suite
- Synthesis using Xilinx Plan Ahead tool & Xilinx Synthesis tool
- Implementation and Data Configuration in Xilinx FPGAs
- CMOS Inverter design using digital flow of Cadence tools
- Schematic Entry and SPICE simulation of MOS differential amplifier



A Two day National Workshop
On

"VLSI Design Laboratory"

13-02-2020 & 14-02-2020
(Thursday & Friday)

Chairman
Dr.A.V.Ramprasad, Principal

Convener & H.O.D - ECE
Dr.V.Kejalakshmi

Coordinators
Dr.N.Janakiraman
Dr.B.Buvaneswari
Mrs.M.Amudha
Mr.D.Anand

Organized by

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

K.L.N.COLLEGE OF ENGINEERING
Pottapalayam - 630 612
Madurai District.
Phone: 0452 2090971, 2090972
URL : www.klnce.edu

ABOUT THE INSTITUTE

K.L.N. College of Engineering has been the first self-financing co-educational Engineering College started in Madurai in 1994. The College has been affiliated to Anna University and approved by All India Council for Technical Education (AICTE). The College is located in the south eastern outskills of Madurai and is 11Km away from Madurai city. The college runs 7 undergraduate engineering programs and 7 Master Programs including M.E. Communication Systems.

DEPARTMENT OF ECE

The Department of ECE was started in 1994. The Department has adequate infrastructure with spacious classrooms, conference halls and well developed nine laboratories having the advanced designing tools like Xilinx Vivado System Edition, Cadence Front-end & Back-end design suites, LabView, MATLAB, ADS, AnSoft, Orcad P-Spice and modernized equipments like Analog discovery kit, Microwave power meter, Spectrum analyzer, Network analyzer. The department initiates the U.G., P.G. & research projects in Embedded Systems through the Centre for Embedded Systems which is based on the collaboration of institution & embedded industry. AICTE, New Delhi has sanctioned fund as under MODROB scheme for modernizing Microwave Lab and DSP lab of this department. The department library has over 1500 books and magazines and journals.

PROGRAM SCHEDULE

DAY-1:-

09:00 - 09:30 – Registration
09:30 - 09:45 – Inauguration
09:45 - 11:00 – Presentation on VLSI FPGA Design Flow
11:00 - 11:15 – Tea Break
11:15 - 12:45 – **Demonstration:** Xilinx Vivado Design Tools and Xilinx System Edition tools like ISE Simulator, Plan Ahead Synthesizer, HLS, Logic Analyzer & FPGA implementation
12:45 - 01:30 – Lunch Break
01:30 - 03:00 – **Hands on –** 8 bit Adders & 4 bit Multipliers using Xilinx tools
03:00 - 04:20 – **Hands on –** ALU, Universal Shift Register & Finite State Machines using Xilinx tools

DAY-2:-

09:10 - 09:45 – Presentation on VLSI ASIC Design Flow
09:45 - 10:30 – Presentation on Cadence Digital Design Suite - Front-end & Back-end Tools
10:30 - 10:45 – Tea Break
10:45 - 11:45 – **Demonstration:** CMOS Inverter design using Cadence Virtuoso tool
11:45 - 12:45 – **Hands on –** Simulation using Cadence Virtuoso tool
12:45 - 01:30 – Lunch Break
01:30 - 03:00 – **Hands on –** Manual/Automatic Layout Generation and Post Layout Extraction
03:00 - 04:10 – **Hands on –** Analyze the power, area and timing
04:10 - 04:20 – Feedback and Conclusion

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REGISTRATION FORM

Name :

Qualification :

Designation:

Experience :

Department:

Organization :

Address for :
Communication

Phone No.:

Mobile No.:

E-mail id:

Accommodation required : Yes ☐ ☐

Date: **Signature of the Applicant**